CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a bulk material of a first conductivity comprising a front side and a back side, wherein said back side of said bulk material is supplied with a first potential;

first wells of said first conductivity formed in said front side of said bulk material, wherein at least one of said first wells is supplied with said first potential;

second wells of said first conductivity formed in said front side of said bulk material, wherein at least one of said second wells is supplied with a second potential which is different than said first potential;

third wells of a second conductivity formed in said front side of said bulk material; and

a first buried layer of said second conductivity extending between said back side of said bulk material and said first, second and third wells, said first buried layer comprising at least one opening therein to electrically connect said bulk material with said at least one of said first wells supplied with said first potential;

wherein said at least one of said second wells supplied with said second potential is electrically isolated from said at least one opening of said first buried layer by at least one of said third wells.

2. The semiconductor device of Claim 1, wherein said first potential is a ground potential, and said second potential is a bias potential.

3. The semiconductor device of Claim 1, further comprising a second buried layer of said first conductivity extending between said first buried layer of said second conductivity and said at least one of said second wells supplied with said second potential, said second buried layer routing said second potential to said at least one of said second wells.

4. The semiconductor device of Claim 1, wherein said first buried layer routes a bias potential to said at least one of said third wells.

5. A semiconductor device comprising:

a bulk material;

p-wells formed in a front side of said bulk material;

n-wells formed in said front side of said bulk material; and

n layers and p layers alternately formed within said bulk material between a back side of said bulk material and said n-wells and p-wells;

wherein said n layers are electrically isolated from one another and respectively route different potentials to selected ones of said n-wells, and wherein said p layers are electrically isolated from one another and respectively route different potentials to selected ones of said p-wells.

6. A semiconductor device comprising:

a bulk material comprising a front side and a back side;

a first well of a first conductivity in said front side of said bulk material;

a second well of said first conductivity in said front side of said bulk material;

a third well of a second conductivity in said front side of said bulk material;

a first buried layer between said back side of said bulk material and said first well, said second well and said third well; and

a second buried layer between said first buried layer and said second well, wherein said third well and said first buried layer electrically isolate said second buried layer and said second well from said first well.

7. The semiconductor device of Claim 6 wherein said first well is electically connected to said bulk material through an opening in said first buried layer.

8. The semiconductor device of Claim 7 wherein said first buried layer is of said second conductivity and wherein said opening is of said first conductivity.

9. The semiconductor device of Claim 6 further comprising:

a fourth well of said second conductivity, said second buried layer being between said first buried layer and said fourth well, wherein said fourth well is electically connected to said first buried layer through an opening in said second buried layer.

10. The semiconductor device of Claim 9 wherein said first buried layer is of said second conductivity, wherein said second buried layer is of said first conductivity and wherein said opening is of said second conductivity.

11. The semiconductor device of Claim 6 further comprising:

a fourth well of said second conductivity;

a fifth well of said first conductivity;

said second buried layer being between said first buried layer and said fourth well and said fifth well; and

a third buried layer between said second buried layer and said fourth well and said fifth well, wherein said fifth well is electrically connected to said second buried layer through an opening in said third buried layer.

12. The semiconductor device of Claim 11 wherein said second buried layer is of said first conductivity, wherein said third buried layer is of said second conductivity and wherein said opening is of said first conductivity.

13. The semiconductor device of Claim 6 wherein said first buried layer is of said second conductivity and wherein said second buried layer is of said first conductivity.

14. A semiconductor device comprising:

a bulk material comprising a front side and a back side;

a first well of a first conductivity in said front side of said bulk material, said first well being supplied a first potential;

a second well of said first conductivity in said front side of said bulk material;

a third well of a second conductivity in said front side of said bulk material;

a first buried layer of said second conductivity between said back side of said bulk material and said first well, said second well and said third well; and

a second buried layer of said first conductivity between said first buried layer and said second well, wherein said second buried layer supplies a second potential to said second well and wherein said first buried layer supplies a third potential to said third well.

15. The semiconductor device of Claim 14 wherein said third well and said first buried layer electrically isolate said first potential from said third potential.

16. The semiconductor device of Claim 14 wherein said first well is supplied with said first potential through an opening in said first buried layer, said opening of said first conductivity.

17. The semiconductor device of Claim 14 further comprising:

a fourth well of said second conductivity, said second buried layer being between said first buried layer and said fourth well, wherein said fourth well is supplied with said third potential through an opening in said second buried layer.

18. The semiconductor device of Claim 17 wherein said opening is of said second conductivity.

19. The semiconductor device of Claim 14 further comprising:

a fourth well of said second conductivity;

a fifth well of said first conductivity;

said second buried layer being between said first buried layer and said fourth well and said fifth well; and

a third buried layer of said second conductivity between said second buried layer and said fourth well and said fifth well, wherein said fifth well is supplied with said second potential through an opening in said third buried layer.

20. The semiconductor device of Claim 19 wherein said opening is of said first conductivity.

21. A semiconductor device comprising:

a bulk material comprising a front side and a back side;

a first well of a first conductivity in said front side of said bulk material;

means for supplying said first well with a first potential;

a second well of said first conductivity in said front side of said bulk material;

a third well of a second conductivity in said front side of said bulk material;

means for supplying a second potential to said second well; and

means for supplying a third potential to said third well, wherein said means for supplying a third potential is between said back side of said bulk material and said first well, said second well and said third well, and wherein said means for supplying a second potential is between said means for supplying a third potential and said second well.

22. A method comprising:

forming a first well of a first conductivity, a second well of said first conductivity, and a third well of a second conductivity in a front side of a bulk material;

forming a first buried layer of said second conductivity between a back side of said bulk material and said first well, said second well and said third well;

forming a second buried layer of said first conductivity between said first buried layer and said second well,

supplying a first potential to said first well;

supplying a second potential to said second well with said second buried layer; and

supplying a third potential to said third well with said first buried layer.

23. The method of Claim 22 further comprising electrically isolating said first potential from said second potential with said third well and said first buried layer.